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54 Method of manufacturing a semiconductor device with an interconnection electrode layer.

57 A method for manufacturing a semiconductor device having a highly reliably interconnection electrode layer (27) is disclosed, which comprises the steps of forming a first material layer (23) on a semiconductor substrate (21), forming a second material layer (24) made of silicon nitride on the first material layer (23), selectively removing the second material layer (24) by a reactive ion etching method using a gas containing hydrogen and carbon-halogen bonds, to form an opening (26a) with a sloped side wall, and selectively removing the first material layer (23) by an etching method permitting the first and second material layers (23, 24) to be etched away, to form an opening (26b) with a sloped side wall.

FIG. 3A

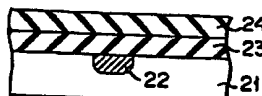


FIG. 3B

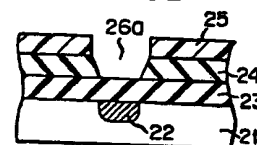


FIG. 3C

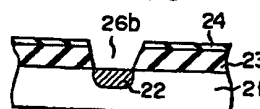
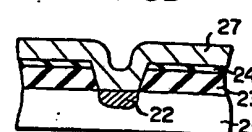


FIG. 3D



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Method for manufacturing a semiconductor device

5 This invention relates to a method for manufacturing a semiconductor device and in particular an improved method for forming thin layers on a semiconductor substrate.

10 Recently, a multi-interconnection structure has more often been adopted with the advent of a high-density and high-integrated version of semiconductor device. One important task in the formation of the multi-interconnection structure is to prevent the disconnection of the interconnection electrode layer due to a possible stepped configuration. An etching technique is used in the formation of such multi-interconnection structure. With a recent advance of
15 a microminiaturization technique the etching technique is shifted from a wet process using a liquid etchant to a dry process utilizing plasma. Recently, a dry etching method has been used in the formation of a contact hole and through hole in an insulating layer as well as the
20 patterning of a metal electrode layer. The dry etching process permits a thin layer such as an insulating layer and metal layer to be formed without undercutting.

25 A step for forming a contact hole by a dry method in an insulating layer on a semiconductor substrate and step for forming an interconnection electrode layer on the insulating layer will be explained by referring to

Figs. 1A and 1B. In Fig. 1A, an active region such as a diffusion layer is formed in a semiconductor substrate and then a contact hole 4 is formed by a dry etching method with a resist film as a mask. The side wall
5 of the contact hole 4 extends vertically as shown in Fig. 1A. If, as shown in Fig. 1B, a metal layer 5, i.e. a first interconnection layer, is formed by a vacuum evaporation or sputtering method on the insulating layer, metal will not be deposited on the side wall of
10 the contact hole 4, resulting in a so-called "disconnection" phenomenon. As a countermeasure against such phenomenon, a method has been proposed in which metal is deposited on a substrate, while heating the substrate, to cause the mobility of the deposited metal atoms to be
15 enhanced to permit adequate metal to be deposited on the side wall of the contact hole 4. According to this method, however, an irregular surface is likely to be formed on the interconnection electrode layer, making it unsuitable for the microminiaturization of the semiconductor structure.
20

The disconnection phenomenon occurs on an interconnection electrode layer on a contact hole, on an interconnection electrode layer on the through hole of the insulating layer between the layers of the multi-
25 interconnection structure, and on an upper interconnection electrode layer on the discontinuity area of a lower interconnection electrode layer.

An object of this invention is to provide a method for manufacturing a semiconductor device for preventing
30 a possible disconnection of an interconnection electrode layer.

Another object of this invention is to provide a semiconductor device having a multi-interconnection structure of high reliability.

35 According to this invention there is provided a method for manufacturing a semiconductor device, comprising the steps of forming a first material layer

on a semiconductor substrate, forming a second material layer made of silicon nitride on the first material layer, selectively removing the second material layer, and selectively removing the first material layer with the second material layer as a mask, characterized in that the second material layer is selectively removed by a reactive ion etching method using a gas containing hydrogen and carbon-halogen bonds, to form an opening with a sloped side wall, and said first material layer is selectively removed by an etching method to form an opening with a sloped side wall, the etching method permitting the first and second material layers to be etched away.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A and 1B are cross-sectional views showing the steps of forming a conventional interconnection electrode layer;

Fig. 2 is a cross-sectional view showing a reactive ion etching apparatus as used in the process of this invention;

Figs. 3A to 3D are cross-sectional views showing the process of one method of this invention;

Figs. 4A to 4E are cross-sectional views showing the process of another method of this invention; and

Figs. 5A to 5E are cross-sectional views showing the process of another method of this invention.

After various research into a dry etching technique, the inventors have discovered that, if with a resist pattern as a mask a silicon nitride layer is subjected to a reactive ion etching using a gas containing hydrogen and carbon-halogen bonds to selectively remove the silicon nitride layer, the side wall of a resultant opening in the silicon nitride layer is sloped with respect to a horizontal plane. This invention is based on this discovery. That is, this discovery is applied

to the formation of an interconnection electrode layer on the material layer with an opening. With the silicon nitride layer whose opening has a sloped side wall as a mask, an underlying material layer is selectively removed by an etching method whereby both the silicon nitride layer and the underlying material layer can be etched away, to automatically form a sloped side wall in a resultant opening in the material layer. If a conductive material is deposited directly on the material layer or on an insulating layer overlying the material layer, followed by patterning, an interconnection electrode layer is formed on or above the opening without producing any disconnection.

The gas containing hydrogen and carbon-halogen bonds as an etchant may be a mixture gas of a hydrogen gas with a gas of CF_4 , C_2F_6 , C_3F_8 , CCl_4 , CH_3Br or the like. A CHF_3 gas may also be used. Where use is made of a gas mixture of a hydrogen gas with a gas containing carbon-halogen bonds, an amount of hydrogen gas is preferably 10 to 40 % based on the whole amount of the gas mixture. In this case, it is possible to obtain a silicon nitride layer whose opening has a sloped side wall with an inclination angle of 60° to 70° .

The reactive ion etching is performed by an apparatus as shown in Fig. 2. A workpiece 14 is placed on one (12b) of a pair of parallel, planar electrodes 12a, 12b which are mounted within an etching chamber 11. The electrode 12b is connected to a high frequency power generator.

As the etching method whereby both the silicon nitride and the underlying material can be etched away, use may be made of any etching method such as a plasma etching, reactive ion etching, sputtering etching, wet etching method, in which a proper etchant is used. For example, a gas mixture of a H_2 gas with a fluorocarbon gas such as CF_4 may be used as an etchant for an underlying material of silicon oxide; a fluoro-carbon

gas such as CF_4 , as an etchant for an underlying material of poly-Si; and a chloro-carbon gas such as CCl_4 as an etchant for an underlying material of aluminium.

5 If a reactive ion etching method using a gas mixture of a H_2 gas with a CF_4 gas as an etchant is adopted with silicon oxide used as the underlying material, the silicon nitride layer is selectively removed by a first
10 etching on an etching device and then a second etching is performed on the same device under the similar conditions by causing an amount of H_2 to be increased or decreased to, for example, 10 to 30 % i.e. an amount
15 permitting both the silicon nitride layer and the underlying material layer to be etched away. As set out in more detail in connection with the following Examples, the method of this invention can be applied to the formation of an interconnection electrode layer on an insulating layer with a contact hole or a through hole or the formation of a second interconnection electrode layer
20 overlying the first interconnection electrode layer having a discontinuity area with an insulating film therebetween. According to this invention an opening such as a contact hole, through hole and discontinuity in the interconnection electrode layer can be formed to
25 have a sloped side wall, preventing a possible disconnection of an interconnection electrode which is formed on the opening. As a result, it is possible to obtain a semiconductor device having a multi-interconnection structure of high reliability.

30 The embodiment of this invention will be explained below by reference to the accompanying drawings.

Example 1

35 As shown in Fig. 3A, a first insulating layer such as a silicon oxide film 23 is wholly coated on a semiconductor substrate 21 in which an active region 22 such as a diode and transistor is formed and then a silicon nitride film 24 is formed by a plasma CVD method

using, for example, SiH_4 and NH_3 . As shown in Fig. 3B, with a resist 25 as a mask a silicon nitride film 24 is etched, by a reactive ion etching method (using a device as shown in Fig. 2), under the conditions of 25 cc/min of CF_4 , 9 cc/min. of H_2 , 0.01 Torr of pressure and 0.25 W/cm^2 of a high frequency power. In this step, a hole 26a is formed in the silicon nitride film 24 and has a taper of 60° to 70° . After the resist 25 is removed, a reactive ion etching is effected. If at this time both the silicon oxide film 23 and nitride film 24 are etched in a mixed gas under the conditions such as 20 cc/min. of CF_4 and 10 cc/min. of H_2 , since a sloped side wall has already been formed in the hole 26a, the hole 26a is widened with the continued etching to form a tapered contact hole 26b as shown in Fig. 3C, which would not otherwise be formed by an ordinary etching with a resist as a mask. When the selective etching of the silicon oxide film 23 is completed, the silicon nitride film 24 is thinly left on the resultant structure, but it may be completely removed dependent upon the etching requirements. As shown in Fig. 3D, an interconnection electrode layer 27 made of, for example, aluminium is formed on the resultant structure. Since in this case the taper is formed on the side wall of the contact hole, no disconnection of the interconnection layer 27 occurs due to a possible stepped configuration. Although, in this Example, the resist 25 is removed after the silicon nitride film 24 is selectively etched, the silicon oxide film 23 may be etched with the resist 25 left as it is.

Example 2

In this Example, this invention is applied to the formation of a through hole in a multi-interconnection structure. As shown in Fig. 4A, an insulating layer 32 is formed on a semiconductor substrate 31 and a first interconnection layer 33 is formed on the insulating layer 32. As shown in Fig. 4B, for example, a silicon

oxide film 34 is formed as an insulating layer and then a silicon nitride film 35 is coated on the surface of the resultant structure. As shown in Fig. 4C, with a resist 36 as a mask a through hole 37a is formed, as in
5 Example 1, in a predetermined area of the silicon nitride film 35. If, as shown in Fig. 4D, etching is effected as in Example 1 after the resist 36 is removed, a tapered through hole 37b is formed in the silicon oxide film (the insulating layer) as in Example 1. As
10 shown in Fig. 4E, a second interconnection layer 38 is formed on the surface of the resultant structure. In this case, no discontinuity occurs due to a possible stepped configuration.

Example 3

15 In this Example, this invention is applied to the formation of an interconnection layer per se. As shown in Fig. 5A, a first interconnection layer 43 made of, for example, poly-Si or aluminium is formed on an insulating layer 42 overlying a semiconductor substrate 41.
20 As shown in Fig. 5B a silicon nitride film 44 is wholly formed on the surface of the resultant structure. As shown in Fig. 5C, with a resist 45 as a mask the silicon nitride film 44 is etched into a predetermined interconnection pattern to provide, for example, a slit 46a. At
25 this time, the silicon nitride film 44 can be etched such that, as in Examples 1 and 2, the slit 46a has a taper on its side wall. If with the silicon nitride film 44 as a mask the interconnection layer 43 is subjected to a reactive ion etching using, for example, a
30 CF₄ gas for poly-Si or a CCl₄ gas for aluminium, a taper is formed on the side wall of a slit 46b of the interconnection layer 43. When an insulating layer 47 is coated on the surface of the resultant structure and then a second interconnection layer 48 is formed on the
35 surface of the insulating layer 47, no discontinuity of the interconnection layer 48 occurs due to a possible stepped configuration.

Claims:

1. A method for manufacturing a semiconductor device comprising a step of forming a first material (23) layer on a semiconductor substrate (21), a step of
5 forming a second material layer (24) made of silicon nitride on the first material layer (23), a first etching step of selectively removing the second material layer (24), and a second etching step of selectively removing the first material layer (23) with the second
10 material layer (24) as a mask, characterized in that said second material layer (24) is selectively removed by a reactive ion etching method using a gas containing hydrogen and carbon-halogen bonds to form an opening (26a) with a sloped side wall, and said first material
15 layer (23) is selectively removed by an etching method to form an opening (26b) with a sloped side wall, said etching method permitting said first and second materials layers (23, 24) to be etched away.

2. A method according to claim 1, wherein said gas
20 containing hydrogen and carbon-halogen bonds is a gas mixture of CF_4 , C_2F_6 , C_3F_8 , CCl_4 or CF_3Br and H_2 or CHF_3 gas.

3. A method according to claim 1, wherein said gas containing hydrogen and carbon-halogen bonds is a gas
25 mixture of CF_4 , C_2F_6 , C_3F_8 , CCl_4 or CF_3Br and H_2 in which the volume of H_2 is 10 to 40 volume percent of the total volume of said gas mixture.

4. A method according to any one of claims 1 to 3 in which said first material layer (23) is a silicon
30 oxide layer and said second etching step is performed by a reactive ion etching method using a gas mixture of a fluorocarbon gas and H_2 gas as an etchant.

5. A method according to any one of claims 1 to 3 in which said first material layer (23) is an aluminium
35 layer and said second etching step is performed by a dry etching method using a chloro-carbon gas as an etchant.

6. A method according to any one of claims 1 to 3,
in which said first material layer (23) is a polycrys-
talline silicon layer and said second etching step is
performed by a dry etching method using a fluorocarbon
gas as an etchant.
- 5

FIG. 1A

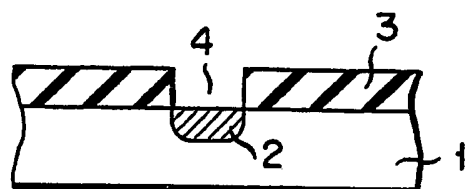


FIG. 1B

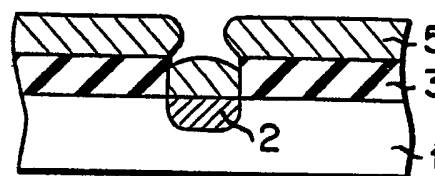


FIG. 3A

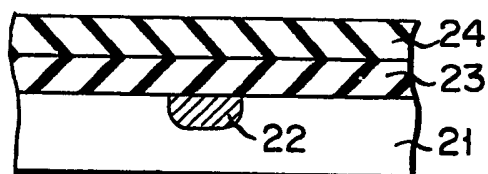


FIG. 3B

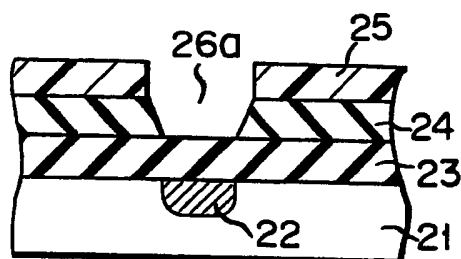


FIG. 3C

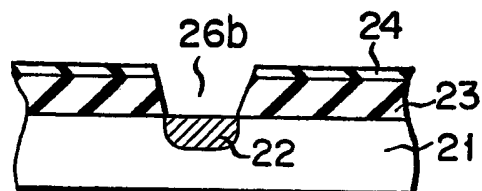


FIG. 3D

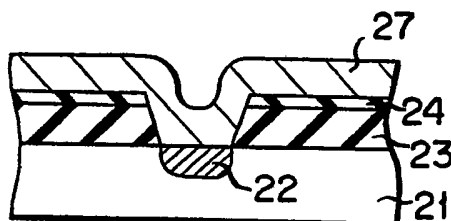


FIG. 2

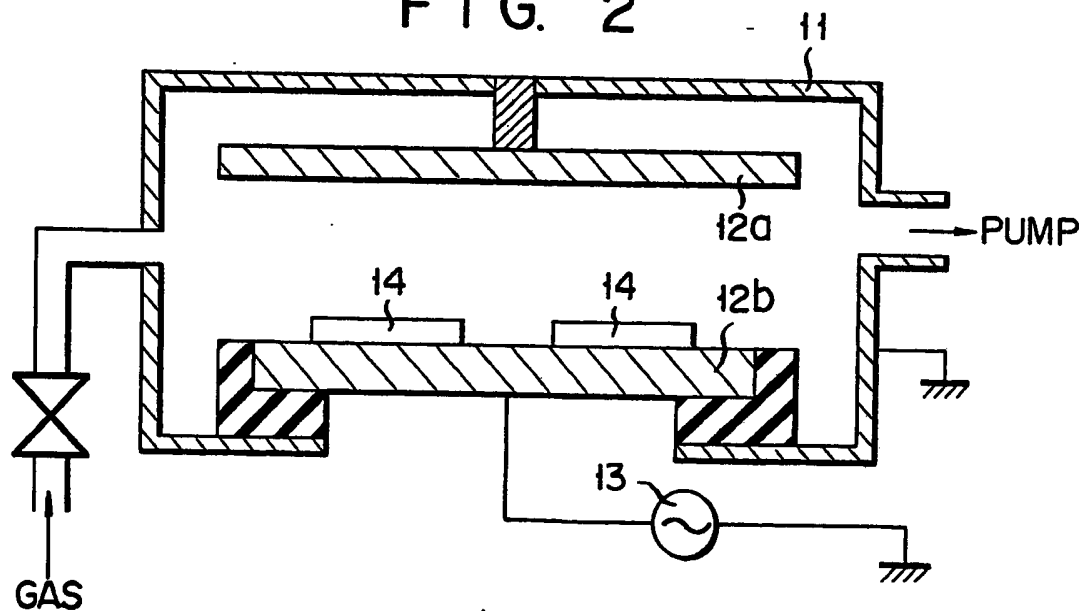


FIG. 4A

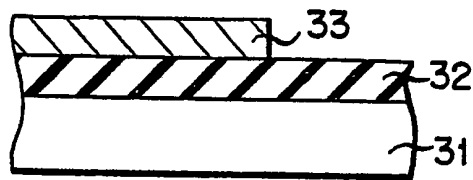


FIG. 5A

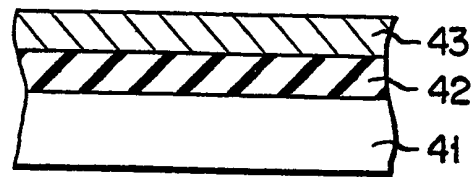


FIG. 4B

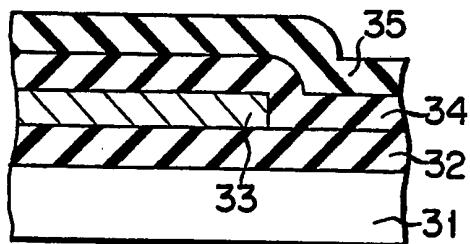


FIG. 5B

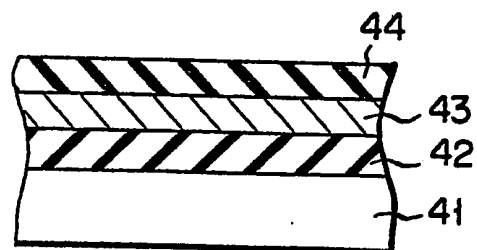


FIG. 4C

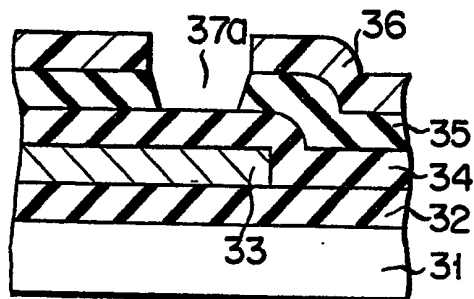


FIG. 5C

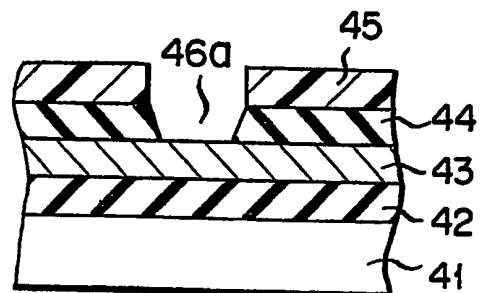


FIG. 4D

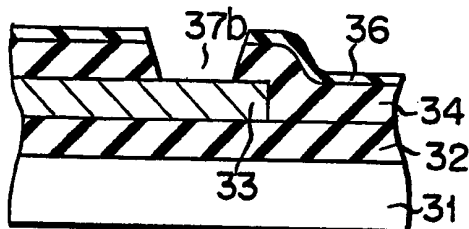


FIG. 5D

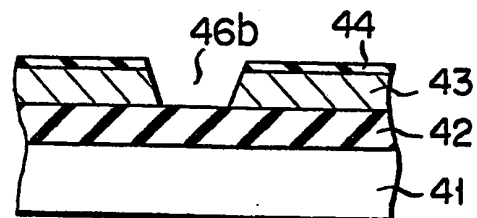


FIG. 4E

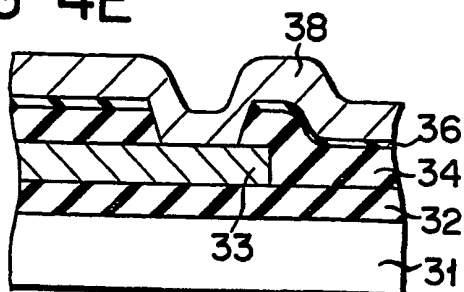


FIG. 5E

